Pb Free Plating Product

CS48N80

70V,87A N-Channel Trench Process Power MOSFET

General Description

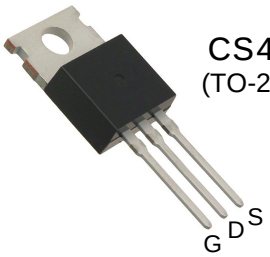
The CS48N80 is N-channel MOS Field Effect Transistor designed for high current switching applications. Rugged E_{AS} capability and ultra low $R_{DS(ON)}$ is suitable for PWM, load switching especially for E-Bike controller applications.

Features

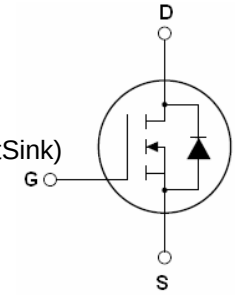
- V_{DS}=70V; I_D=87A@ V_{GS}=10V;
  $R_{DS(ON)}$<5.8mΩ @ V_{GS}=10V
- Special Designed for E-Bike Controller Application
- Ultra Low On-Resistance
- High UIS and UIS 100% Test

Application

- 48V E-Bike Controller Applications
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply



CS48N80
(TO-220 HeatSink)



Schematic Diagram

V_{DSS} = 70V

I_{DSS} = 87A

$R_{DS(ON)}$ = 5.5mΩ

Table 1. Absolute Maximum Ratings (TA=25℃)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage (V_{GS}=0V)	70	V
V_{GS}	Gate-Source Voltage (V_{DS}=0V)	±25	V
$I_{D\ (DC)}$	Drain Current (DC) at Tc=25℃	87	A
$I_{D\ (DC)}$	Drain Current (DC) at Tc=100℃	60.9	A
$I_{DM\ (pluse)}$	Drain Current-Continuous@ Current-Pulsed **(Note 1)**	348	A
dv/dt	Peak Diode Recovery Voltage	30	V/ns
P_D	Maximum Power Dissipation(Tc=25℃)	111	W
	Derating Factor	0.74	W/℃
E_{AS}	Single Pulse Avalanche Energy **(Note 2)**	552	mJ
T_J,T_{STG}	Operating Junction and Storage Temperature Range	-55 To 175	℃

Notes 1.Repetitive Rating: Pulse width limited by maximum junction temperature

2.E_{AS} condition:T_J=25℃,V_{DD}=33V,V_G=10V,I_D=48A

Table 2. Thermal Characteristic

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance,Junction-to-Case	1.35	℃/W

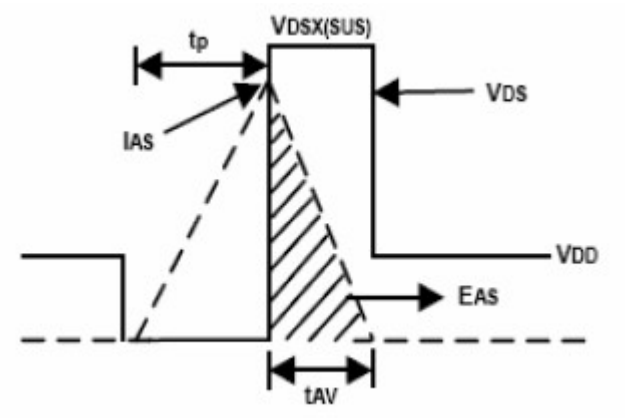
Table 3. Electrical Characteristics (TA=25℃unless otherwise noted)

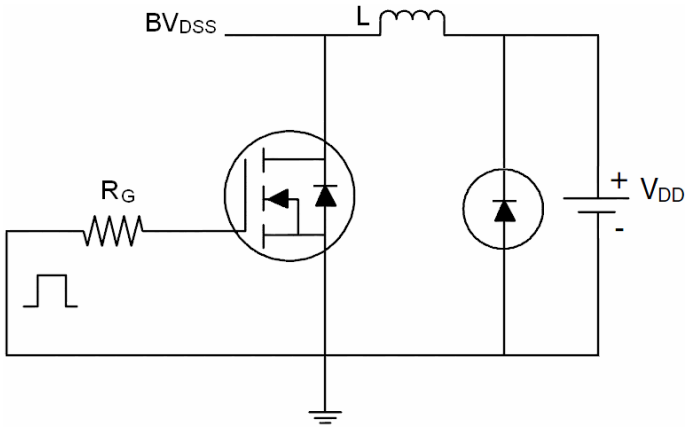
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V I_D=250μA	70			V
I_{DSS}	Zero Gate Voltage Drain Current(Tc=25℃)	V_{DS}=68V,V_{GS}=0V			1	μA
I_{DSS}	Zero Gate Voltage Drain Current(Tc=125℃)	V_{DS}=68V,V_{GS}=0V			10	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±25V,V_{DS}=0V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	2		4	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=10V, I_D=40A		5.5	5.8	mΩ
Dynamic Characteristics						
g_{FS}	Forward Transconductance	V_{DS}=10V,I_D=40A		28		S
C_{iss}	Input Capacitance	V_{DS}=25V,V_{GS}=0V, f=1.0MHz		3200		pF
C_{oss}	Output Capacitance			350		pF
C_{rss}	Reverse Transfer Capacitance			320		pF
Q_g	Total Gate Charge	V_{DS}=50V,I_D=40A, V_{GS}=10V		76.1		nC
Q_{gs}	Gate-Source Charge			14.9		nC
Q_{gd}	Gate-Drain Charge			31.6		nC
Switching Times						
$t_{d(on)}$	Turn-on Delay Time	V_{DD}=30V,I_D=2A,R_L=15Ω V_{GS}=10V,R_G=2.5Ω		12		nS
t_r	Turn-on Rise Time			14		nS
$t_{d(off)}$	Turn-Off Delay Time			25		nS
t_f	Turn-Off Fall Time			30		nS
Source-Drain Diode Characteristics						
I_{SD}	Source-Drain Current(Body Diode)			87		A
I_{SDM}	Pulsed Source-Drain Current(Body Diode)			348		A
V_{SD}	Forward on Voltage**(Note 1)**	T_J=25℃,I_{SD}=40A,V_{GS}=0V		0.8	0.95	V
t_{rr}	Reverse Recovery Time**(Note 1)**	T_J=25℃,I_F=75A di/dt=100A/μs		45		nS
Q_{rr}	Reverse Recovery Charge**(Note 1)**			90		nC
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible(turn-on is dominated by L_S+L_D)				

Notes 1.Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 1.5%, R_G=25Ω, Starting T_J=25℃

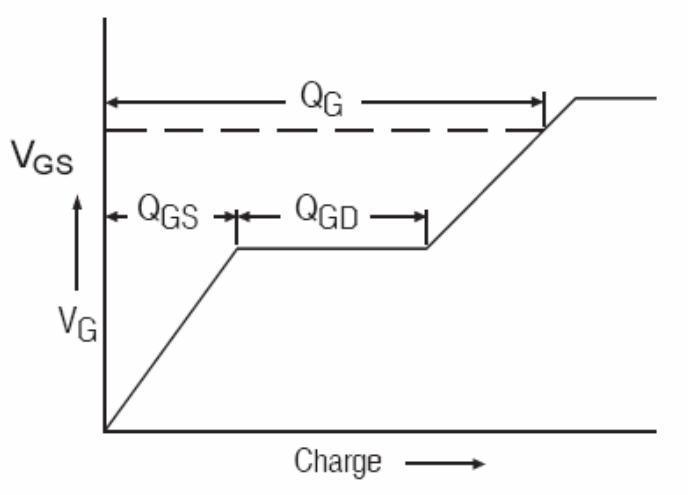
Test Circuit

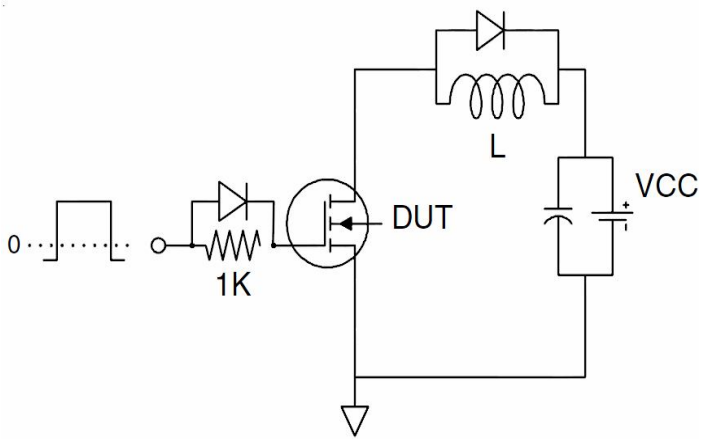
1）E_{AS} Test Circuits



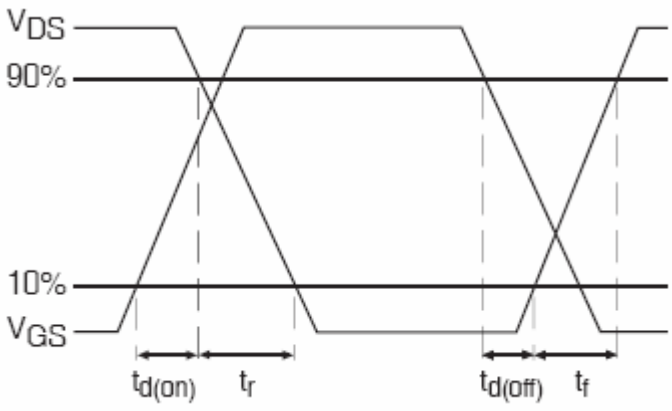


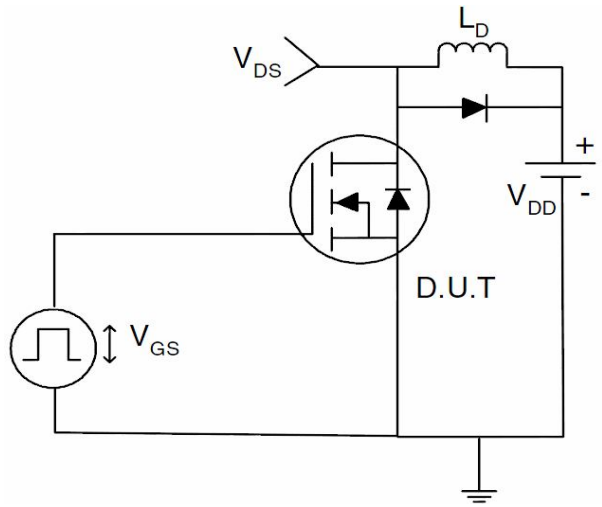
2）Gate charge Test Circuit:





3）Switch Time Test Circuit:





TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)

Figure1. Safe Operating Area

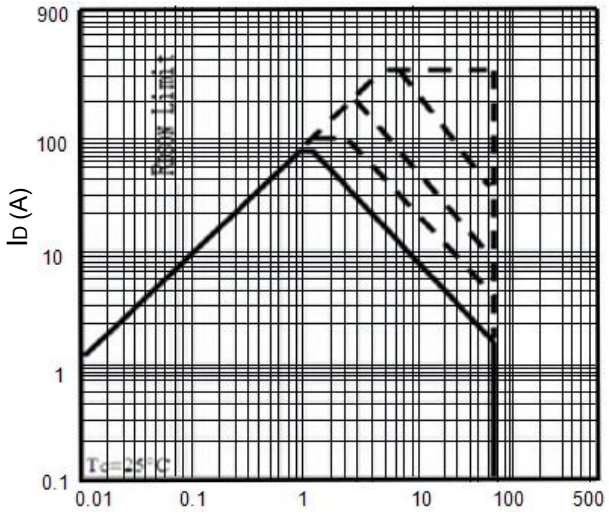


Figure2. Source-Drain Diode Forward Voltage

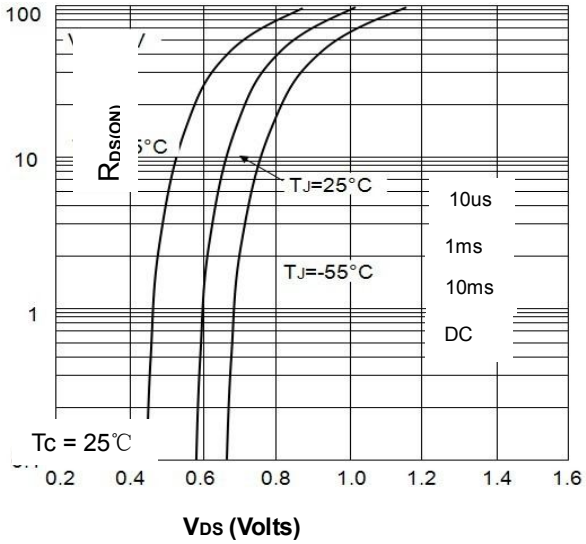


Figure3. Output Characteristics

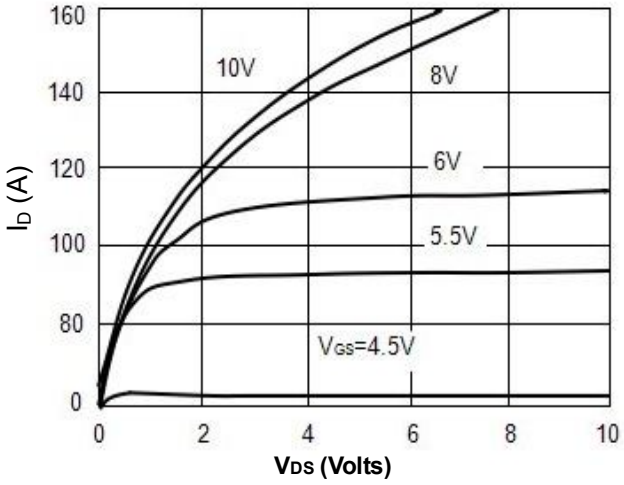


Figure4. Transfer Characteristics

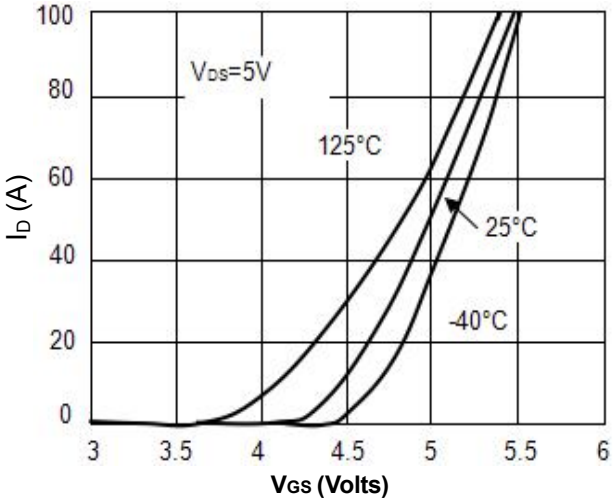


Figure5. Static Drain-Source On Resistance

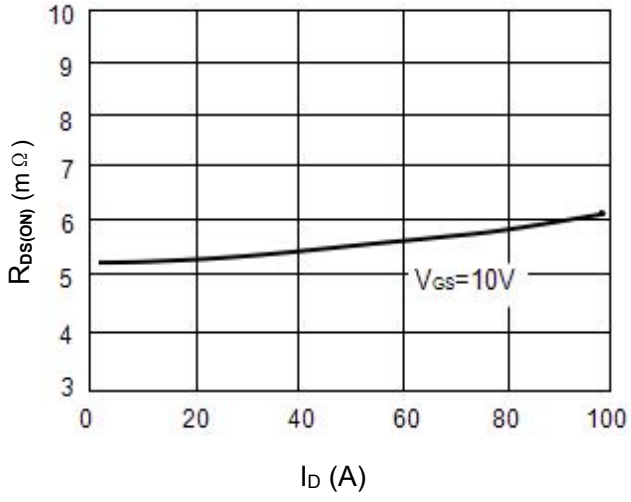


Figure6. $R_{DS(ON)}$ vs Junction Temperature

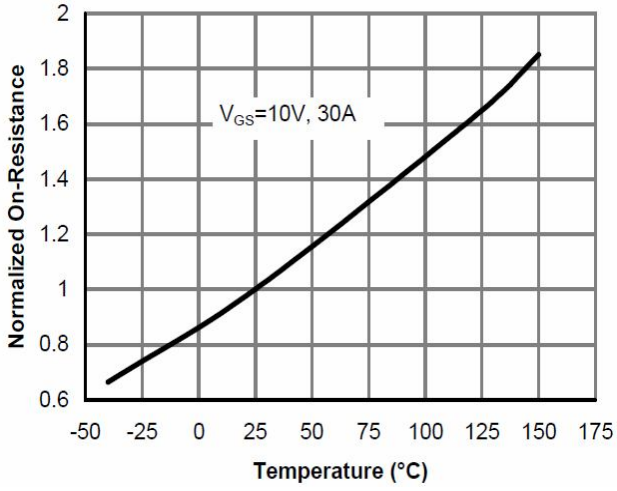


Figure7. BV_{DSS} vs Junction Temperature

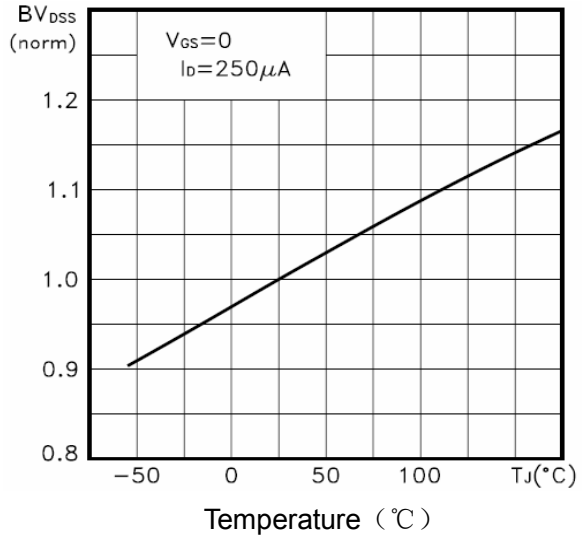


Figure8. $V_{GS(th)}$ vs Junction Temperature

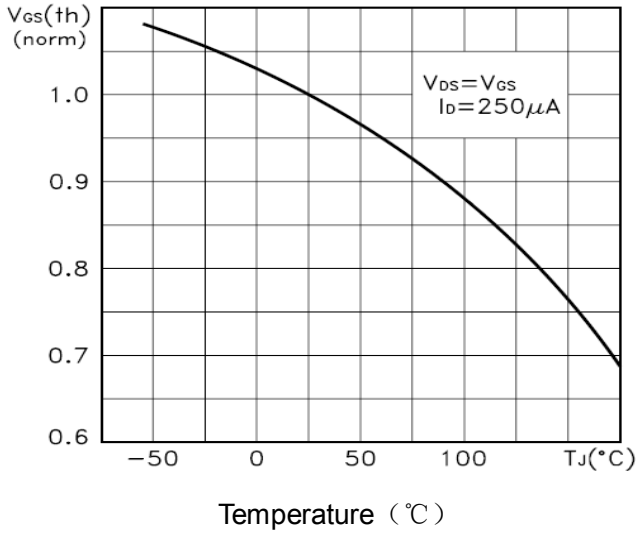


Figure9. Gate Charge Waveforms

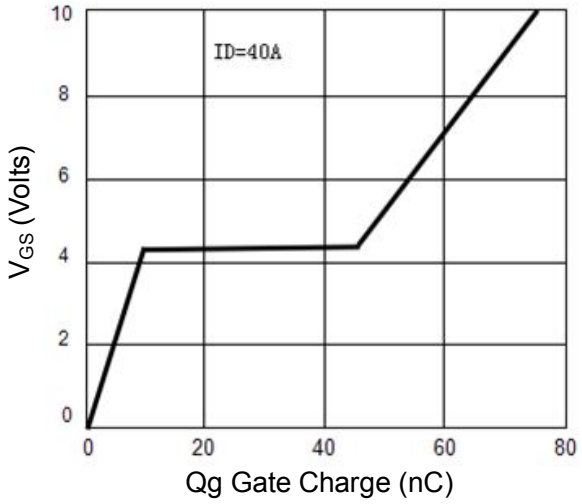


Figure10. Capacitance

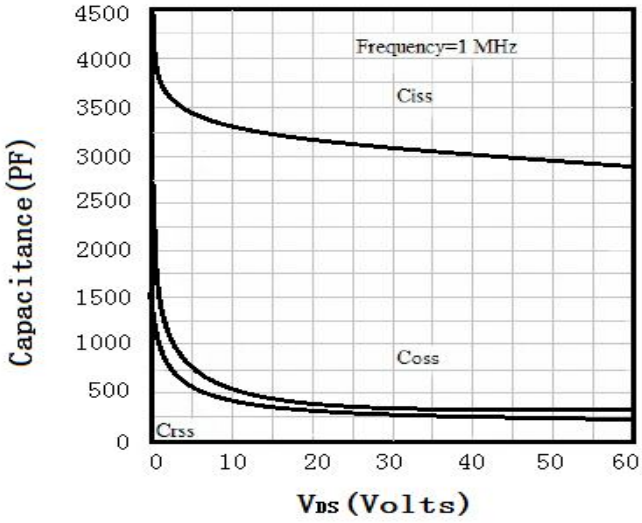


Figure11. Normalized Maximum Transient Thermal Impedance