

Pb Free Plating Product

DK48N80



70V,87A N-Channel Trench Process Power MOSFET

General Description

The DK48N80 is N-channel MOS Field Effect Transistor designed for high current switching applications. Rugged E_{AS} capability and ultra low $R_{DS(ON)}$ is suitable for PWM, load switching especially for E-Bike controller applications.

Features

- $V_{DS}=70V$; $I_D=87A @ V_{GS}=10V$;
 $R_{DS(ON)} < 5.8m\Omega @ V_{GS}=10V$
- Special Designed for E-Bike Controller Application
- Ultra Low On-Resistance
- High UIS and UIS 100% Test

Application

- 48V E-Bike Controller Applications
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply



Schematic Diagram

$$V_{DSS} = 70V$$

$$I_{DSS} = 87A$$

$$R_{DS(ON)} = 5.5m\Omega$$

Table 1. Absolute Maximum Ratings (TA=25°C)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage ($V_{GS}=0V$)	70	V
V_{GS}	Gate-Source Voltage ($V_{DS}=0V$)	± 25	V
$I_{D(DC)}$	Drain Current (DC) at $T_c=25^\circ C$	87	A
$I_{D(DC)}$	Drain Current (DC) at $T_c=100^\circ C$	60.9	A
$I_{DM(pluse)}$	Drain Current-Continuous@ Current-Pulsed (Note 1)	348	A
dv/dt	Peak Diode Recovery Voltage	30	V/ns
P_D	Maximum Power Dissipation($T_c=25^\circ C$)	111	W
	Derating Factor	0.74	W/°C
E_{AS}	Single Pulse Avalanche Energy (Note 2)	552	mJ
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 175	°C

Notes 1.Repetitive Rating: Pulse width limited by maximum junction temperature

2.EAS condition: $T_J=25^\circ C, V_{DD}=33V, V_G=10V, I_D=48A$

Table 2. Thermal Characteristic

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.35	$^{\circ}\text{C}/\text{W}$

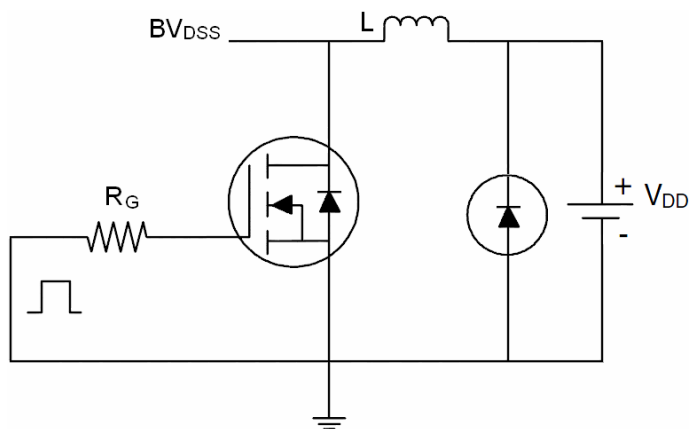
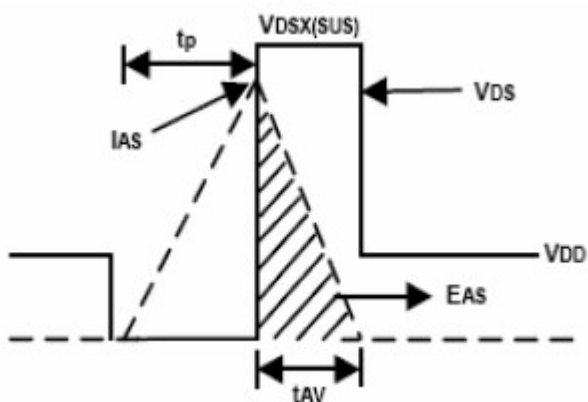
Table 3. Electrical Characteristics (TA=25 $^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V I _D =250μA	70			V
I _{DSS}	Zero Gate Voltage Drain Current(Tc=25℃)	V _{DS} =68V,V _{GS} =0V			1	μA
I _{DSS}	Zero Gate Voltage Drain Current(Tc=125℃)	V _{DS} =68V,V _{GS} =0V			10	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±25V,V _{DS} =0V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} ,I _D =250μA	2		4	V
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =10V, I _D =40A		5.5	5.8	mΩ
Dynamic Characteristics						
g _{FS}	Forward Transconductance	V _{DS} =10V,I _D =40A		28		S
C _{iss}	Input Capacitance	V _{DS} =25V,V _{GS} =0V, f=1.0MHz		3200		pF
C _{oss}	Output Capacitance			350		pF
C _{rss}	Reverse Transfer Capacitance			320		pF
Q _g	Total Gate Charge	V _{DS} =50V,I _D =40A, V _{GS} =10V		76.1		nC
Q _{gs}	Gate-Source Charge			14.9		nC
Q _{gd}	Gate-Drain Charge			31.6		nC
Switching Times						
t _{d(on)}	Turn-on Delay Time	V _{DD} =30V,I _D =2A,R _L =15Ω V _{GS} =10V,R _G =2.5Ω		12		nS
t _r	Turn-on Rise Time			14		nS
t _{d(off)}	Turn-Off Delay Time			25		nS
t _f	Turn-Off Fall Time			30		nS
Source-Drain Diode Characteristics						
I _{SD}	Source-Drain Current(Body Diode)			87		A
I _{SDM}	Pulsed Source-Drain Current(Body Diode)			348		A
V _{SD}	Forward on Voltage ^(Note 1)	T _J =25℃,I _{SD} =40A,V _{GS} =0V		0.8	0.95	V
t _{rr}	Reverse Recovery Time ^(Note 1)	T _J =25℃,I _F =75A di/dt=100A/μs		45		nS
Q _{rr}	Reverse Recovery Charge ^(Note 1)			90		nC
t _{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible(turn-on is dominated by L _S +L _D)				

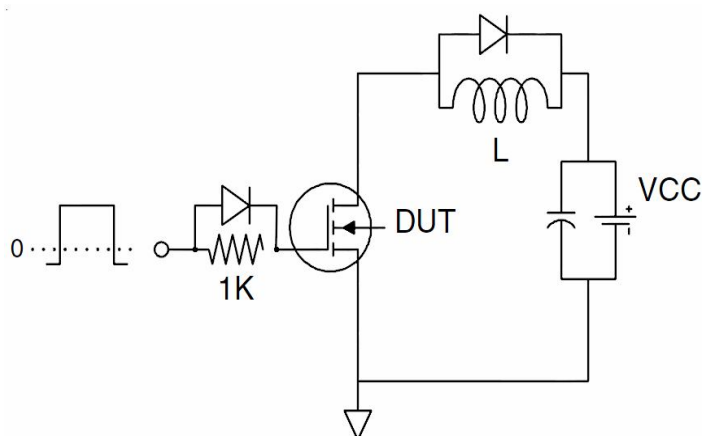
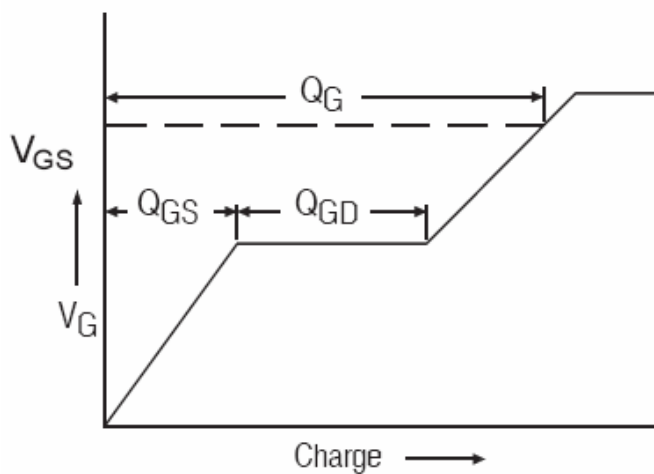
Notes 1. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 1.5\%$, $R_G=25\Omega$, Starting $T_J=25^{\circ}\text{C}$

Test Circuit

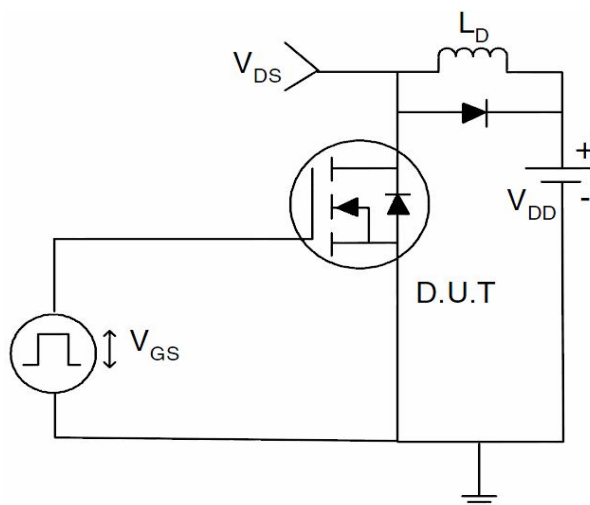
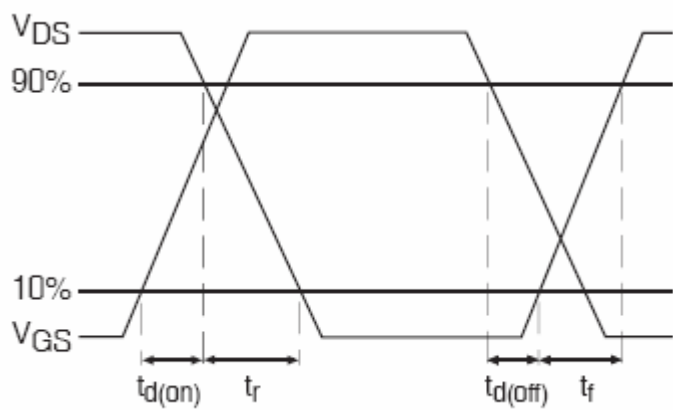
1) E_{AS} Test Circuits



2) Gate charge Test Circuit:



3) Switch Time Test Circuit:



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)

Figure1. Safe Operating Area

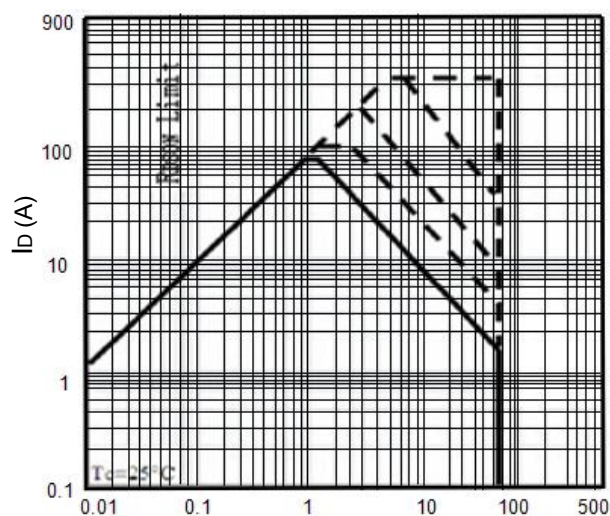


Figure2. Source-Drain Diode Forward Voltage

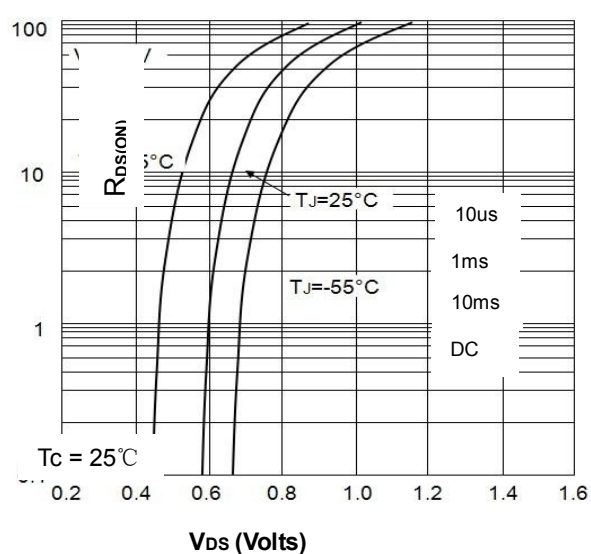


Figure3. Output Characteristics

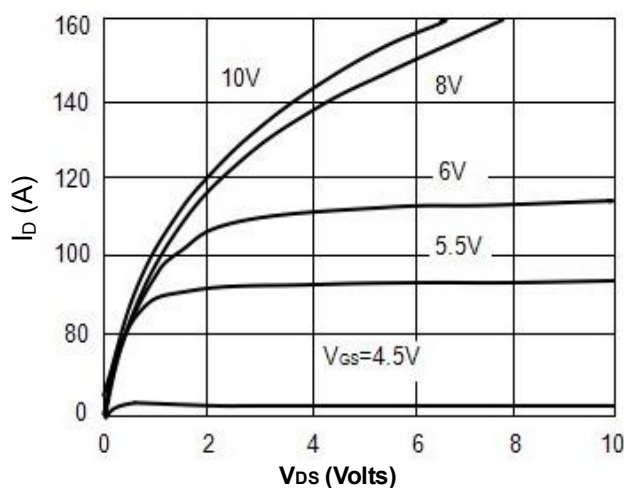


Figure4. Transfer Characteristics

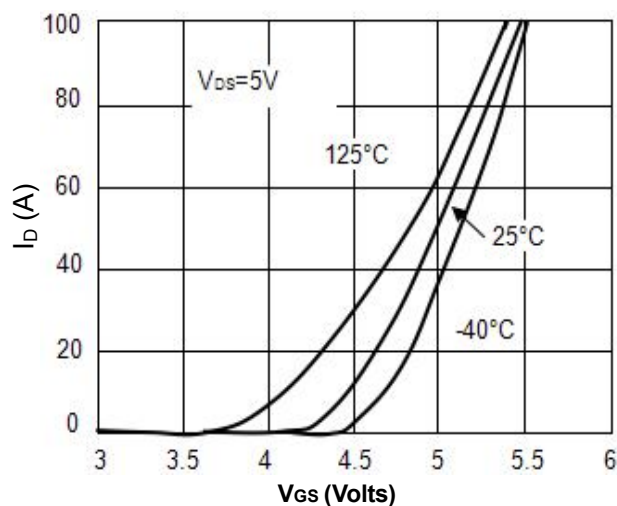


Figure5. Static Drain-Source On Resistance

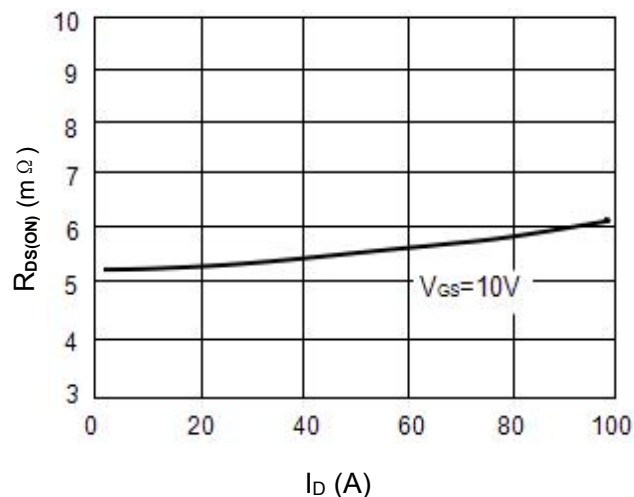


Figure6. $R_{DS(ON)}$ vs Junction Temperature

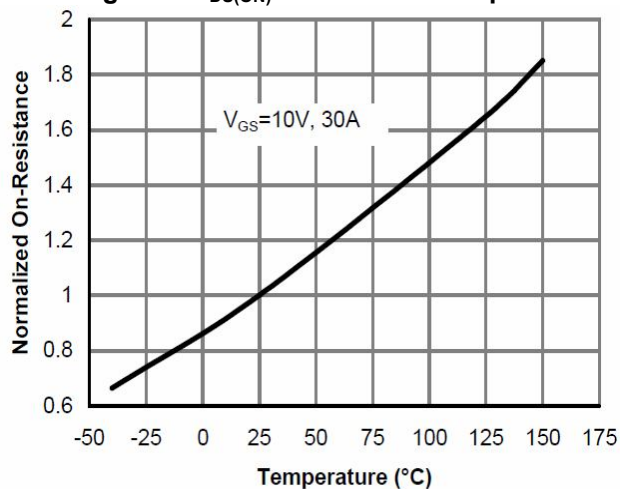


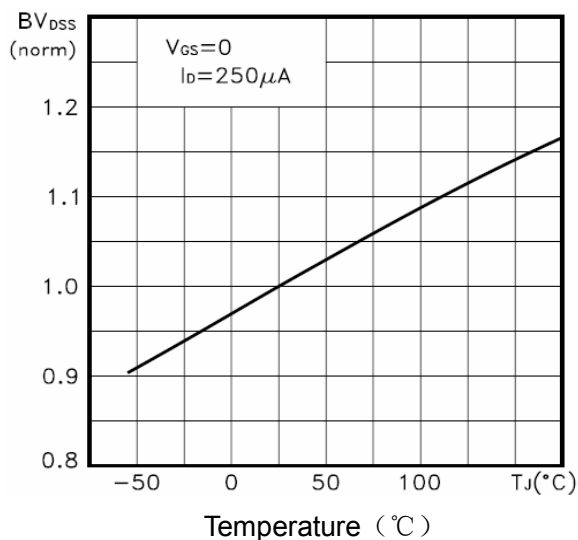
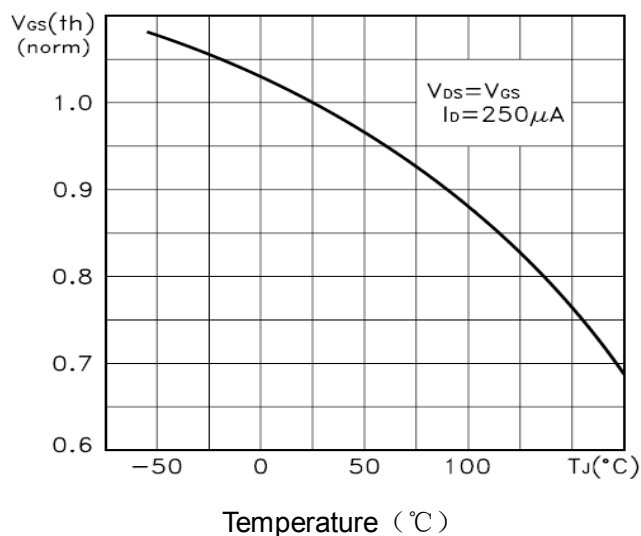
Figure7. BV_{DSS} vs Junction TemperatureFigure8. $V_{GS(th)}$ vs Junction Temperature

Figure9. Gate Charge Waveforms

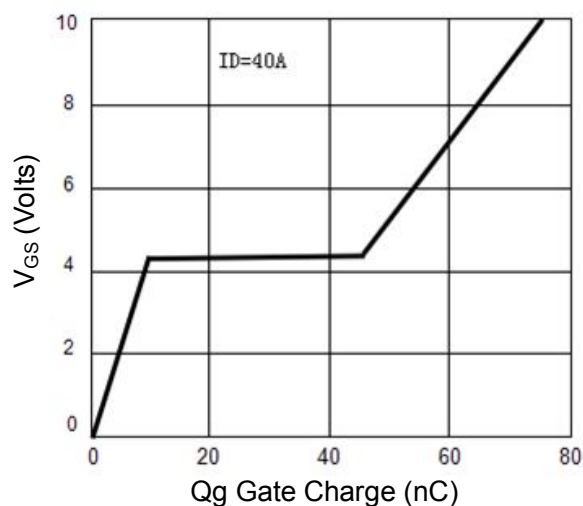


Figure10. Capacitance

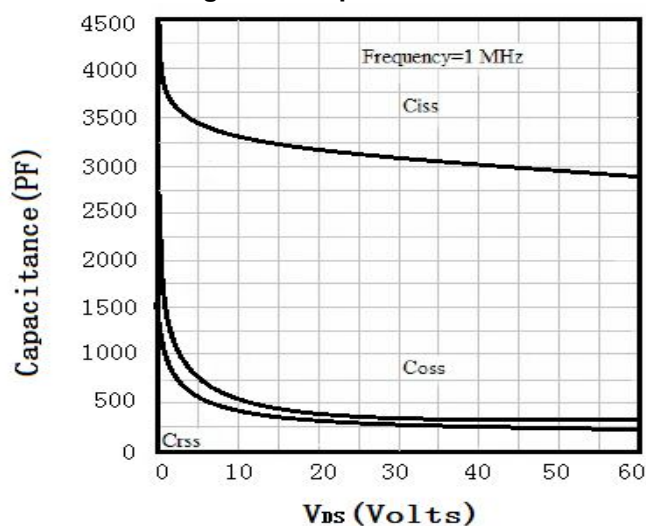


Figure11. Normalized Maximum Transient Thermal Impedance

