

Pb Free Plating Product

IRF3205



N-Channel Trench Process Power MOSFET Transistor

General Description

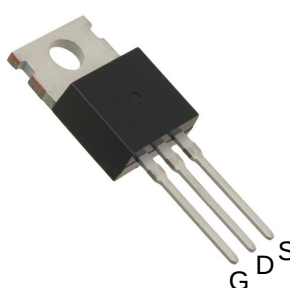
The IRF3205 is N-channel MOS Field Effect Transistor designed for high current switching applications. Rugged EAS capability and ultra low $R_{DS(ON)}$ is suitable for PWM, load switching.

Features

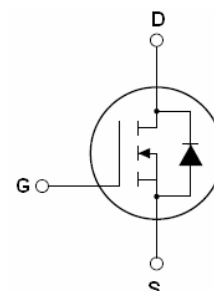
- $V_{DS}=55V$; $I_D=105A$ @ $V_{GS}=10V$;
 $R_{DS(ON)} < 6.0m\Omega$ @ $V_{GS}=10V$
- Ultra Low On-Resistance
- High UIS and UIS 100% Test

Application

- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply
- Inverter Application



TO-220CB Top View



Schematic Diagram

$$V_{DS} = 55 V$$

$$I_D = 105 A$$

$$R_{DS(ON)} = 5.0 m\Omega$$

Table 1. Absolute Maximum Ratings (TA=25°C)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage ($V_{GS}=0V$)	55	V
V_{GS}	Gate-Source Voltage ($V_{DS}=0V$)	± 25	V
$I_D (DC)$	Drain Current (DC) at $T_c=25^\circ C$	105	A
$I_D (DC)$	Drain Current (DC) at $T_c=100^\circ C$	100	A
$I_{DM (pluse)}$	Drain Current-Continuous@ Current-Pulsed (Note 1)	420	A
dv/dt	Peak Diode Recovery Voltage	30	V/ns
P_D	Maximum Power Dissipation($T_c=25^\circ C$)	139	W
	Derating Factor	0.926	W/°C
E_{AS}	Single Pulse Avalanche Energy (Note 2)	625	mJ
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 175	°C

Notes 1.Repetitive Rating: Pulse width limited by maximum junction temperature

2.EAS condition: $T_J=25^\circ C$, $V_{DD}=40V$, $V_G=10V$, $R_G=25\Omega$

Table 2. Thermal Characteristic

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.08	$^{\circ}\text{C}/\text{W}$

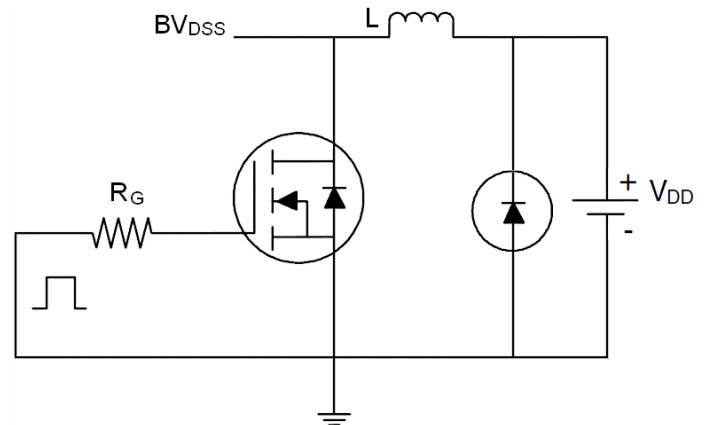
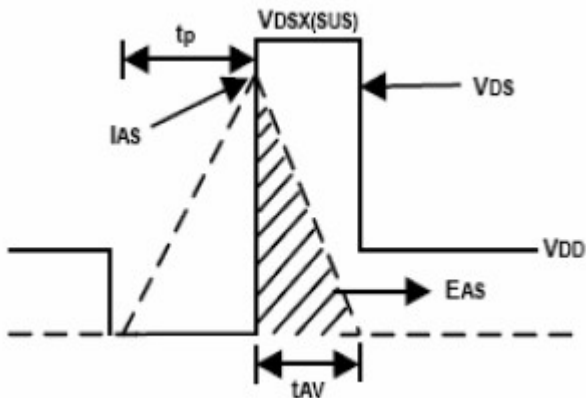
Table 3. Electrical Characteristics (TA=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V I _D =250μA	55			V
I _{DSS}	Zero Gate Voltage Drain Current(Tc=25℃)	V _{DS} =55V,V _{GS} =0V			1	μA
I _{DSS}	Zero Gate Voltage Drain Current(Tc=125℃)	V _{DS} =55V,V _{GS} =0V			1	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V,V _{DS} =0V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} ,I _D =250μA	2		4	V
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =10V, I _D =40A		5.0	6.0	mΩ
Dynamic Characteristics						
g _{FS}	Forward Transconductance	V _{DS} =25V,I _D =40A	25			S
C _{iss}	Input Capacitance	V _{DS} =25V,V _{GS} =0V, f=1.0MHz		5905		PF
C _{oss}	Output Capacitance			905		PF
C _{rss}	Reverse Transfer Capacitance			548		PF
Q _g	Total Gate Charge	V _{DS} =30V,I _D =30A, V _{GS} =10V		94		nC
Q _{gs}	Gate-Source Charge			18		nC
Q _{gd}	Gate-Drain Charge			25		nC
Switching Times						
t _{d(on)}	Turn-on Delay Time	V _{DD} =30V,I _D =2A,R _L =15Ω V _{GS} =10V,R _G =2.5Ω		15		nS
t _r	Turn-on Rise Time			18		nS
t _{d(off)}	Turn-Off Delay Time			31		nS
t _f	Turn-Off Fall Time			38		nS
Source-Drain Diode Characteristics						
I _{SD}	Source-drain Current(Body Diode)			105		A
I _{SDM}	Pulsed Source-Drain Current(Body Diode)			420		A
V _{SD}	Forward On Voltage ^(Note 1)	T _J =25℃,I _{SD} =40A,V _{GS} =0V		0.87	0.95	V
t _{rr}	Reverse Recovery Time ^(Note 1)	T _J =25℃,I _F =75A di/dt=100A/μs		56		nS
Q _{rr}	Reverse Recovery Charge ^(Note 1)			113		nC
t _{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible(turn-on is dominated by L _S +L _D)				

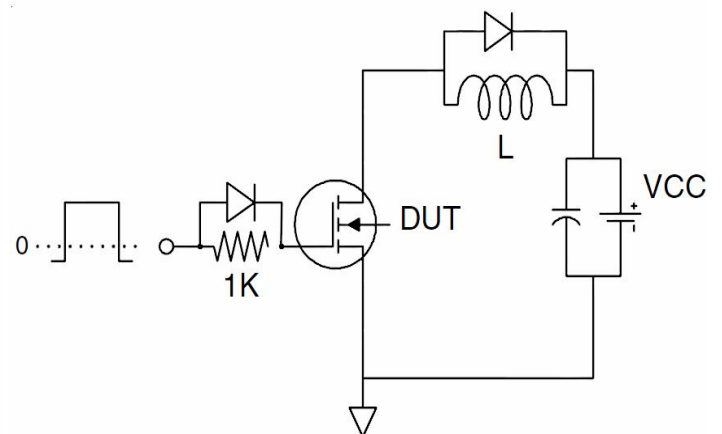
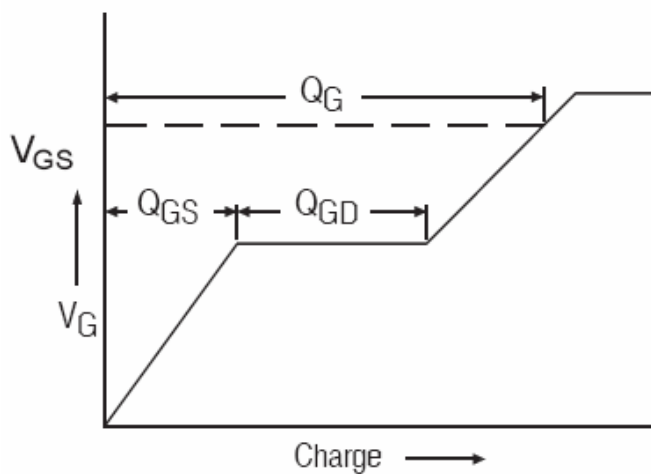
Notes 1. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 1.5\%$, $R_G=25\Omega$, Starting $T_J=25^{\circ}\text{C}$

Test Circuit

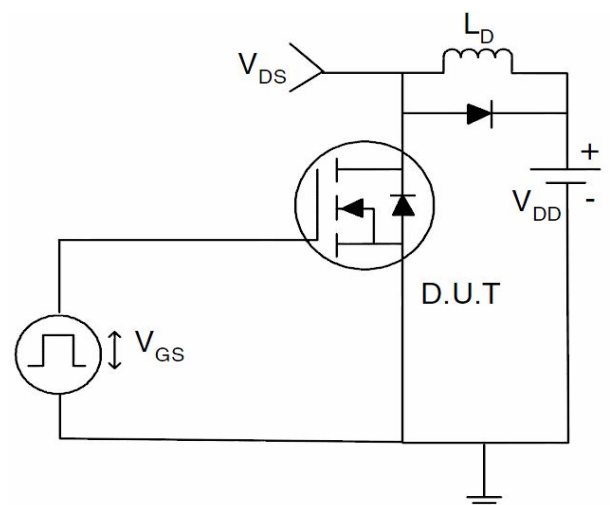
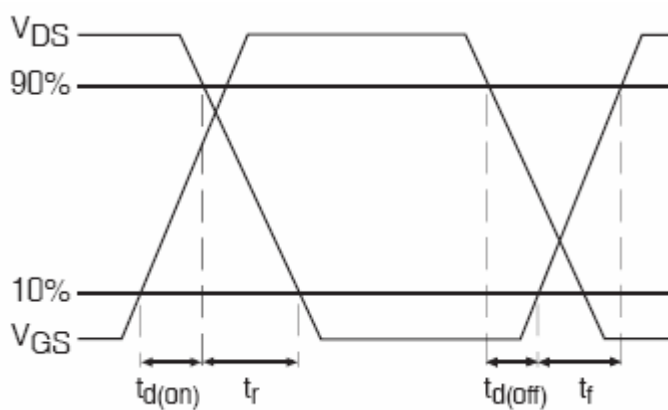
1) E_{AS} Test Circuits



2) Gate Charge Test Circuit:



3) Switch Time Test Circuit:



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)

Figure1. Output Characteristics

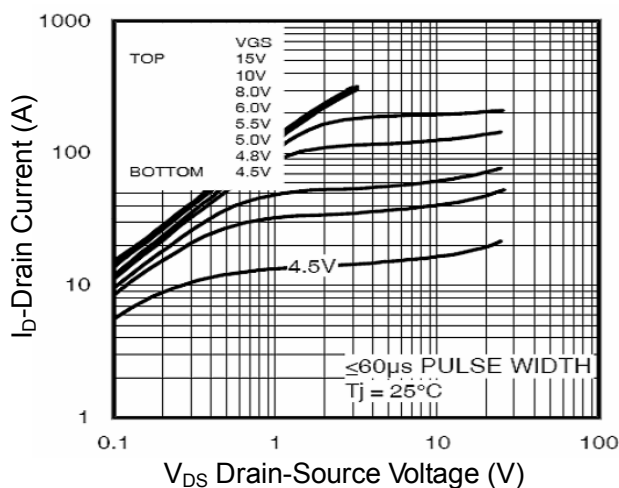


Figure2. Transfer Characteristics

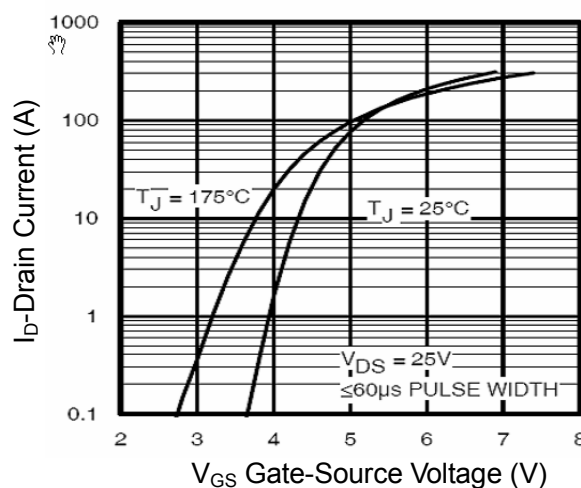


Figure3. Rdson Vs Drain Current

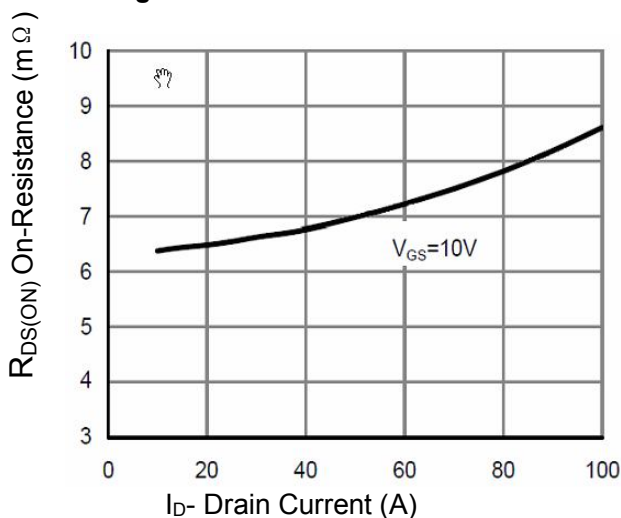


Figure4. Rdson Vs Junction

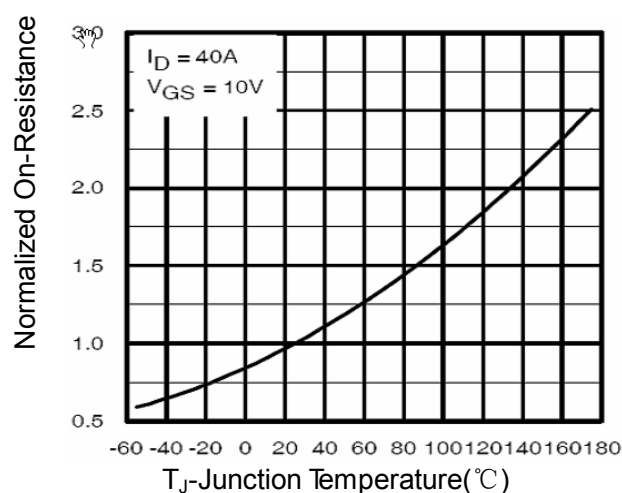


Figure5. Gate Charge

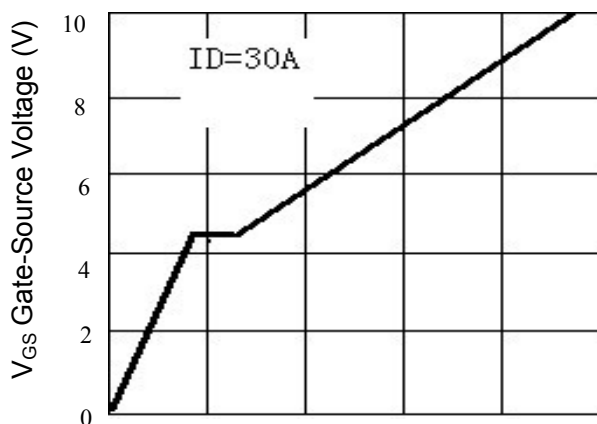


Figure6. Source-Drain Diode Forward

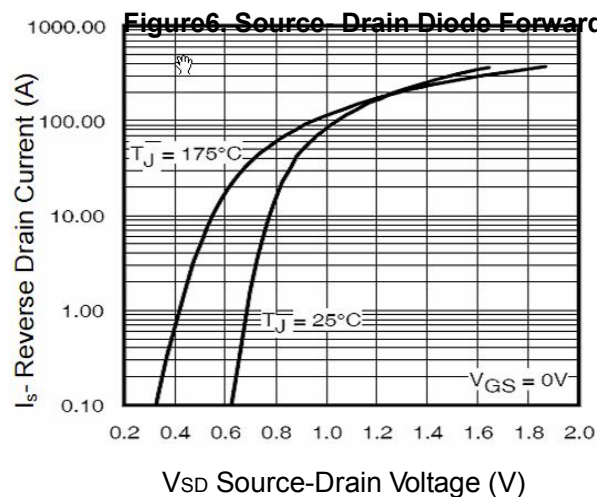


Figure7. Capacitance vs Vds

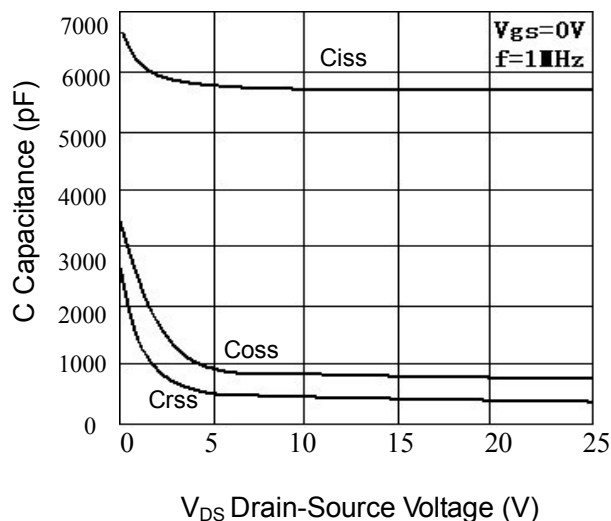


Figure8. Safe Operation Area

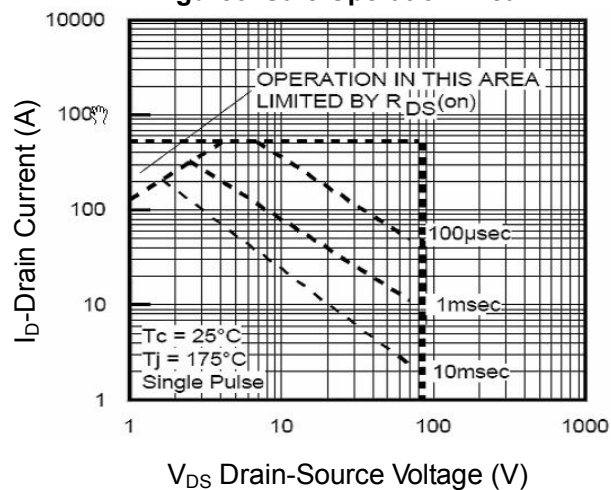


Figure9. BVDSS vs Junction Temperature

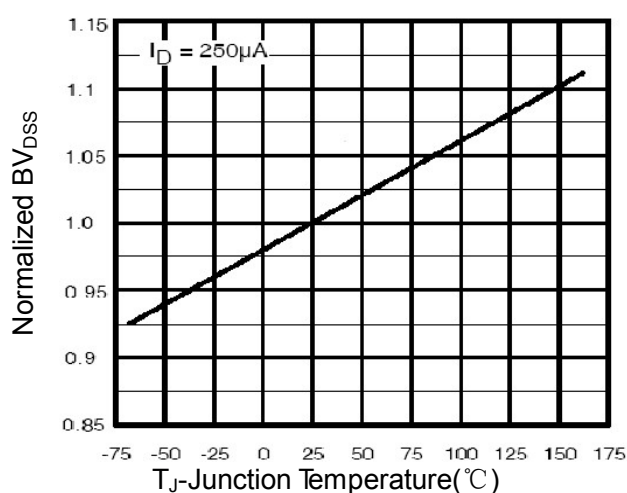


Figure10. VGS(th) vs Junction Temperature

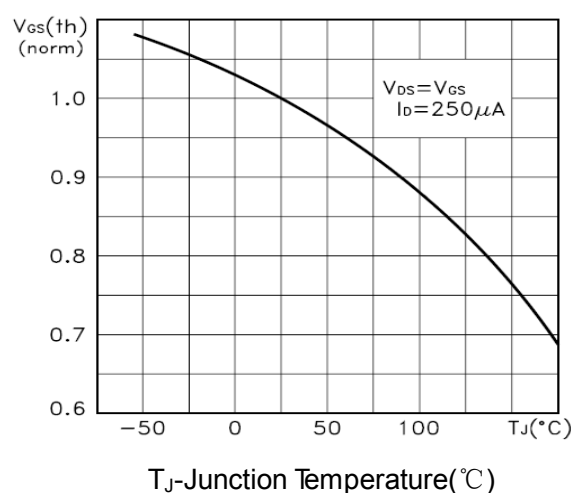


Figure11. Normalized Maximum Transient Thermal Impedance

