

Pb Free Plating Product

TSU45N60



45A,60V Typical N-Channel Trench Power MOSFET

General Description

The TSU45N60 is N-channel MOS Field Effect Transistor designed for high current switching applications. Rugged EAS capability and ultra low $R_{DS(ON)}$ is suitable for PWM.

Features

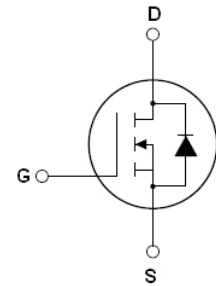
- $V_{DS}=60V$; $I_D=45A@V_{GS}=10V$;
 $R_{DS(ON)}<14\text{ m}\Omega @V_{GS}=10V$
- Ultra Low On-Resistance
- High UIS and UIS 100% Test

Application

- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply
- Inverter/Amplifier Application
- Motor Control Application



G D S
TO-251 Top View



Schematic Diagram

$$V_{DSS} = 60\text{ V}$$

$$I_{DSS} = 45\text{ A}$$

$$R_{DS(ON)} = 11\text{ m}\Omega$$

Table 1. Absolute Maximum Ratings ($T_A=25^\circ\text{C}$)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage ($V_{GS}=0V$)	60	V
V_{GS}	Gate-Source Voltage ($V_{DS}=0V$)	± 25	V
$I_{D(DC)}$	Drain Current (DC) at $T_c=25^\circ\text{C}$	45	A
$I_{D(DC)}$	Drain Current (DC) at $T_c=100^\circ\text{C}$	32	A
$I_{DM(pulse)}$	Drain Current-Continuous@ Current-Pulsed (Note 1)	180	A
P_D	Maximum Power Dissipation($T_c=25^\circ\text{C}$)	55	W
E_{AS}	Single Pulse Avalanche Energy (Note 2)	182	mJ
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 175	$^\circ\text{C}$

Notes 1.Repetitive Rating: Pulse width limited by maximum junction temperature

2.EAS condition: $T_J=25^\circ\text{C}, V_{DD}=30V, V_G=10V, R_G=25\Omega$

Table 2. Thermal Characteristic

Symbol	Parameter	Value	Unit
R _{θJC}	Thermal Resistance, Junction-to-Case	2.7	°C/W

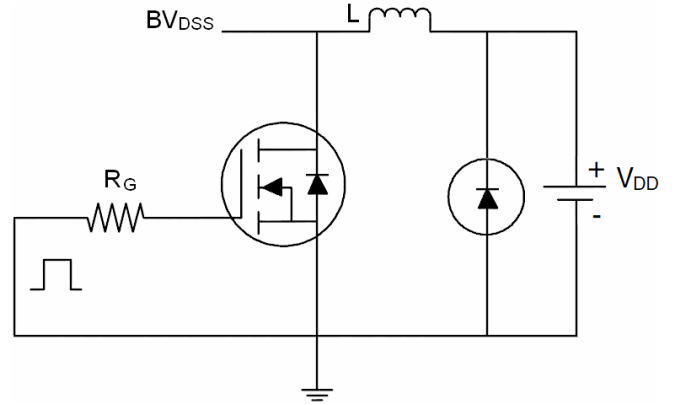
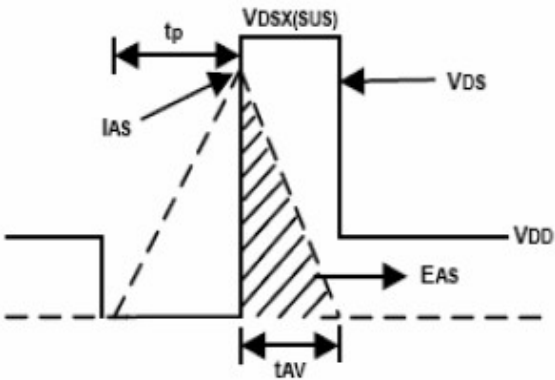
Table 3. Electrical Characteristics (TA=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	60			V
I _{DSS}	Zero Gate Voltage Drain Current(Tc=25°C)	V _{DS} =60V, V _{GS} =0V			1	μA
I _{DSS}	Zero Gate Voltage Drain Current(Tc=100°C)	V _{DS} =60V, V _{GS} =0V			5	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±25V, V _{DS} =0V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	2		4	V
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =10V, I _D =40A		11	14	mΩ
Dynamic Characteristics						
g _{FS}	Forward Transconductance	V _{DS} =10V, I _D =15A	18			S
C _{iss}	Input Capacitance	V _{DS} =25V, V _{GS} =0V f=1.0MHz		1659		PF
C _{oss}	Output Capacitance			276		PF
C _{rss}	Reverse Transfer Capacitance			128		PF
Q _g	Total Gate Charge	V _{DS} =30V, I _D =15A V _{GS} =10V		37.6		nC
Q _{gs}	Gate-Source Charge			6.7		nC
Q _{gd}	Gate-Drain Charge			10		nC
Switching Times						
t _{d(on)}	Turn-on Delay Time	V _{DS} =30V, R _L =2.5Ω V _{GS} =10V, R _G =3Ω		6		nS
t _r	Turn-on Rise Time			6.9		nS
t _{d(off)}	Turn-Off Delay Time			12.5		nS
t _f	Turn-Off Fall Time			14.8		nS
Source-Drain Diode Characteristics						
I _{SD}	Source-Drain Current(Body Diode)			45		A
I _{SDM}	Pulsed Source-Drain Current(Body Diode)			180		A
V _{SD}	Forward On Voltage ^(Note 1)	T _J =25°C, I _{SD} =1A, V _{GS} =0V		0.74	1	V
t _{rr}	Reverse Recovery Time ^(Note 1)	T _J =25°C, I _F =15A di/dt=100A/μs		27		nS
Q _{rr}	Reverse Recovery Charge ^(Note 1)			30		nC
t _{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible(turn-on is dominated by L _S +L _D)				

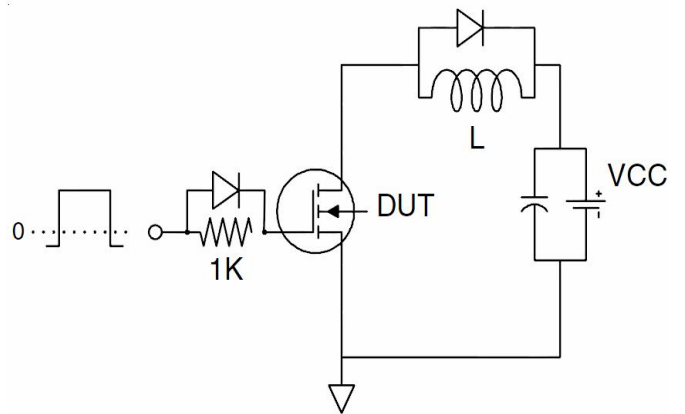
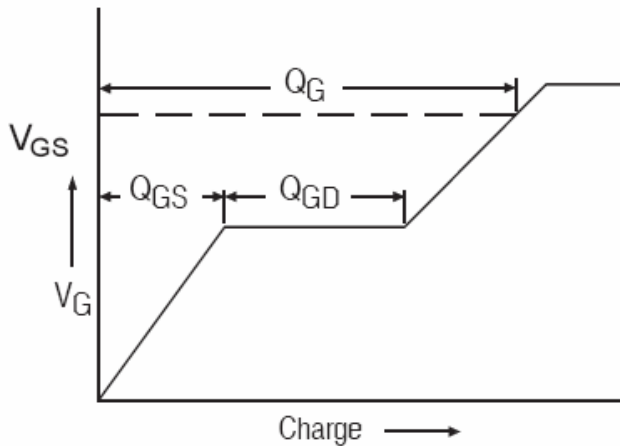
Notes 1. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 1.5%, Starting T_J=25°C

Test Circuit

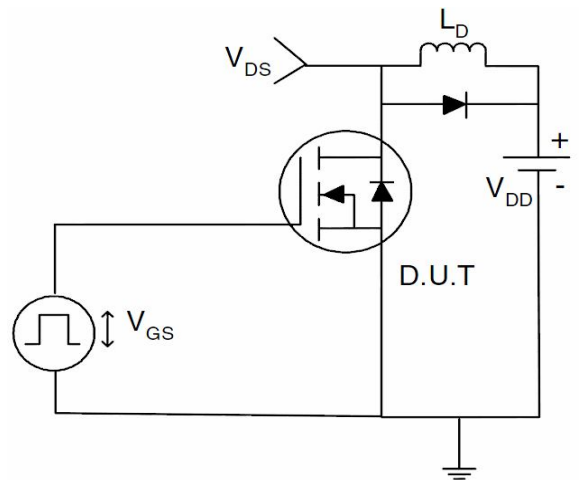
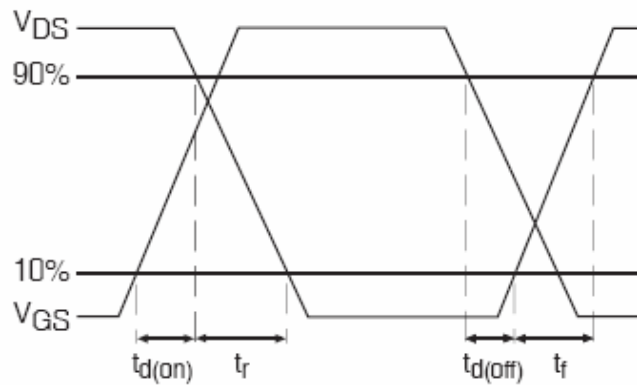
1) EAS Test Circuits



2) Gate Charge Test Circuit:



3) Switch Time Test Circuit:



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)

Figure1. Safe Operating Area

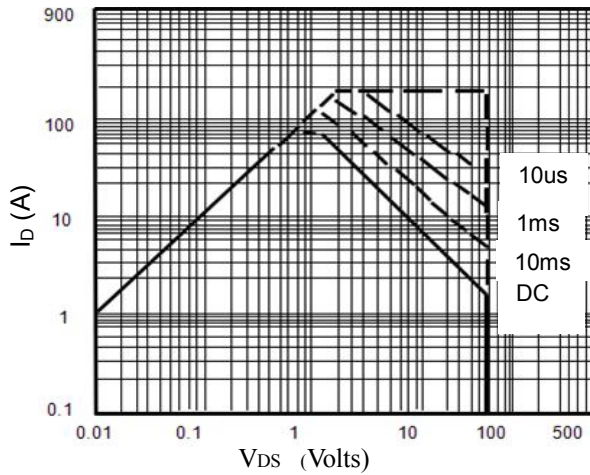


Figure2. Source-Drain Diode Forward Voltage

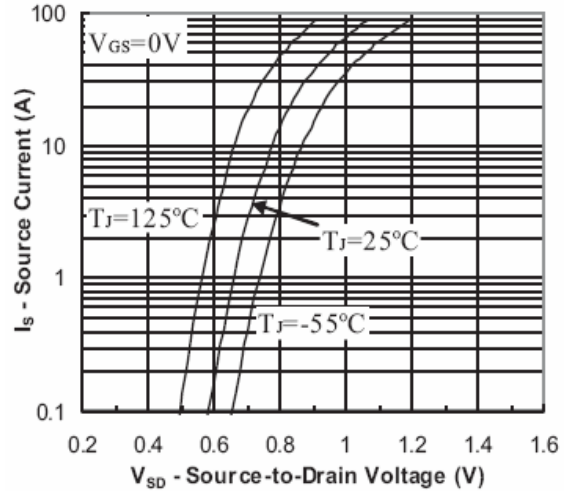


Figure3. Output Characteristics

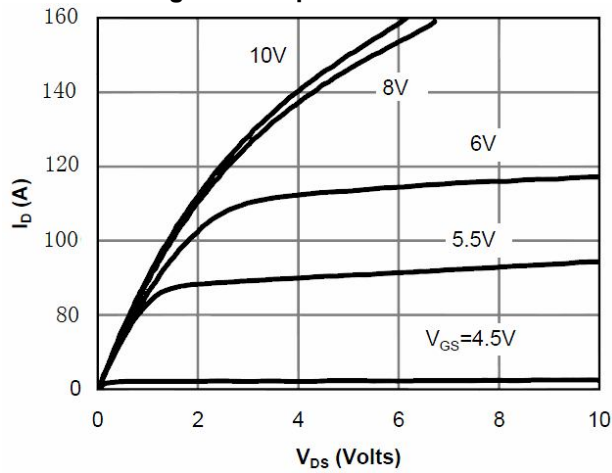


Figure4. Transfer Characteristics

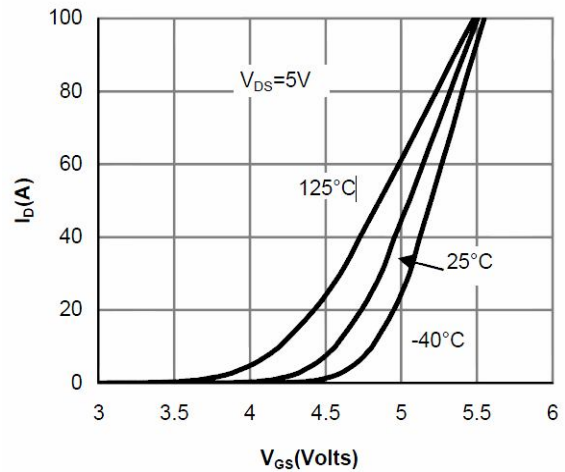


Figure5. Static Drain-Source On Resistance

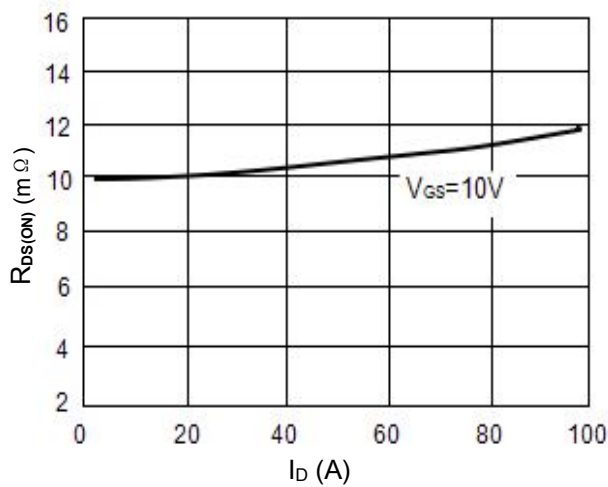


Figure6. $R_{DS(ON)}$ vs Junction Temperature

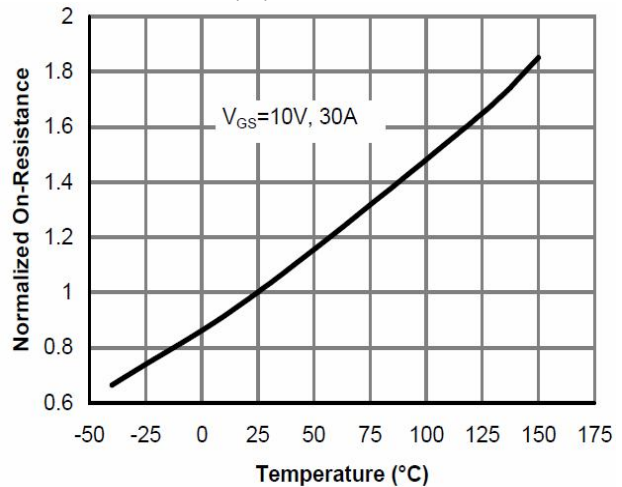


Figure7. BV_{DSS} vs Junction Temperature

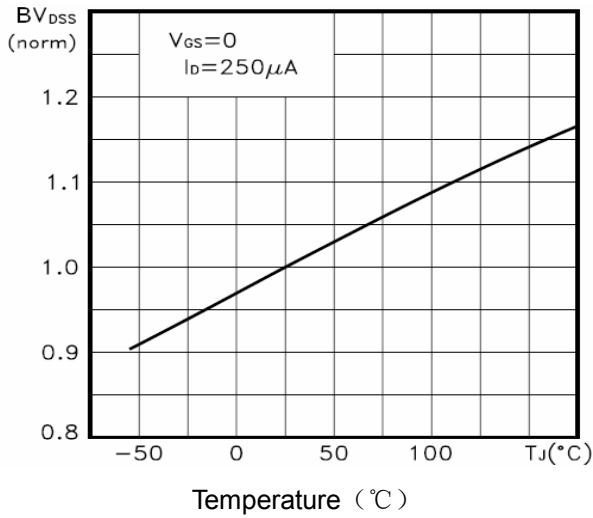


Figure8. $V_{GS(th)}$ vs Junction Temperature

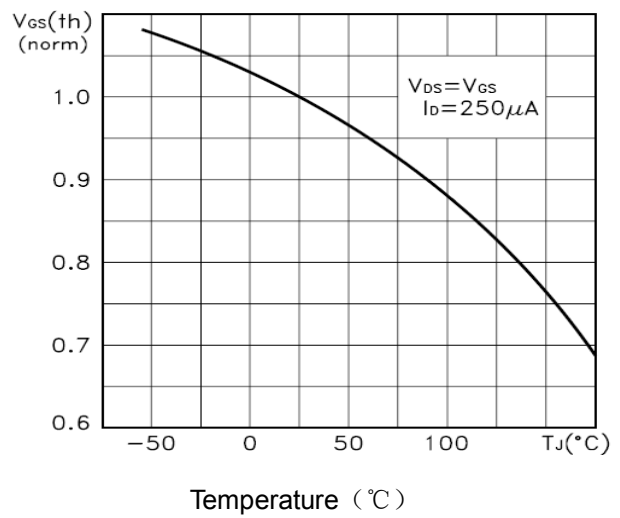


Figure9. Gate Charge Waveforms

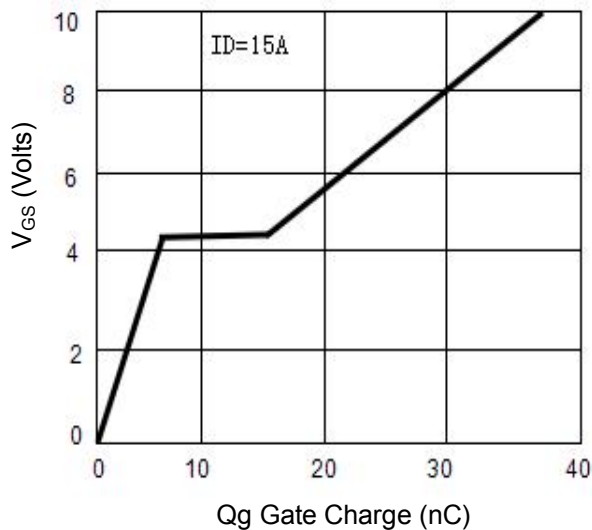


Figure10. Capacitance

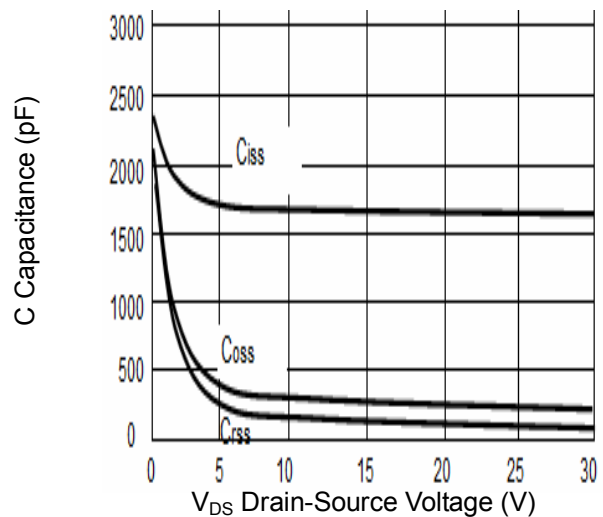


Figure11. Normalized Maximum Transient Thermal Impedance

